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FPGA IMPLEMENTATION OF ADVANCED UART CONTROLLER USING VHDL

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ABSTRACT

As the specific interface chip (ASICs) will cause waste of resources and increased cost. Particularly in the field of electronic design, SOC technology is recently becoming increasingly mature. This situation results in the requirement of realizing the whole system function in a single or a very few chips. Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback of parallel communication and emerges effectively in many applications for long distance communication as it reduces the signal distortion because of its simple structure. The UART implemented with VHDL language can be integrated into the FPGA to achieve compact, stable and reliable data transmission. This paper presents implementation of advanced UART with configurable baud rate.

KEYWORDS: Universal Asynchronous Receiver Transmitter, Serial Receiver, Interrupt Identification Register